Sustainable Semiconductor Additive Manufacturing of Micro and Nanoelectronics

Ahmed Busnaina, William Lincoln Smith Professor, Distinguished University Professor and Director of the NSF Nanoscale Science and Engineering Center for High-rate Nanomanufacturing, Northeastern University, Boston, MA

and

Founder and Chief Technical Officer, Nano OPS, Inc.,
Burlington, MA

www.nanomanufacturing.us, www.nano-ops.us

- Introduction
- Additive Mfg. Using Directed Assembly-based Processes
- Applications in Advanced Packaging
  - Printing of metal, fan out, and resistors
  - Printing of dielectrics and capacitors
  - Printing passive, and active devices and logic gates
  - Scalable and fully automated Fab-in-a-Box
- Summary

A Semiconductor Foundry in a Box

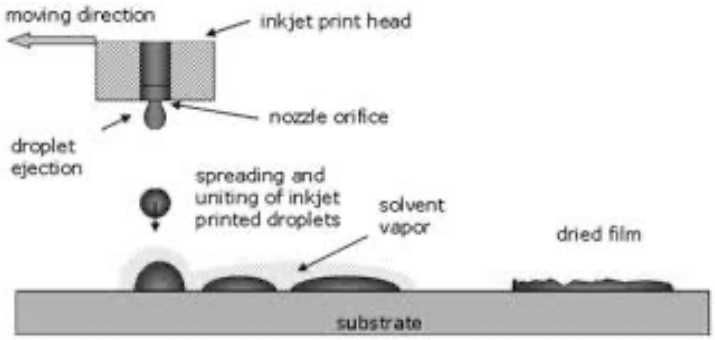
- On demand chips in a few hours
- No etching, chemical reactions, or vacuum
- Secure (trusted) foundry (from zero to full trust).
- 100 times less cost
- 100 times faster than conventional fabrication
- 1000 times reduction in materials use
- 1000 times faster than 3D printing
- 25 nm to 1000 microns feature size demonstrated
- eliminating 100s of process steps

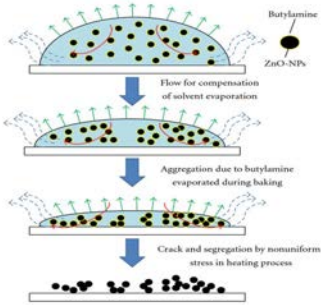
Semiconductor Foundry in a Box

Patented new technology (directed assembly-based printing) to print circuits at the nano and microscale funded by NSF and DoD.

How does directed assembly-based printing work?

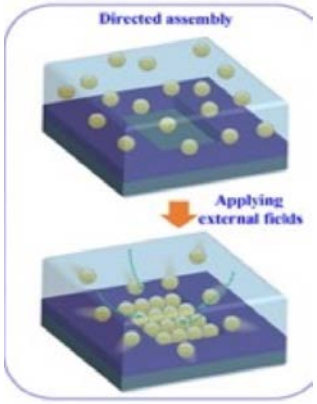
Inkjet printing

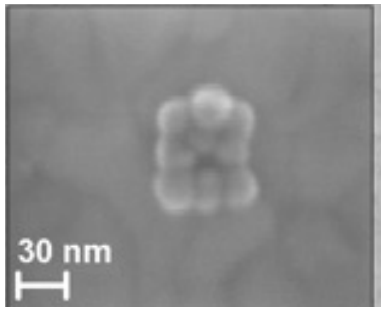




- **Directs a droplet** toward a substrate to form a pattern using many (dots) limiting pattern resolution and fidelity.
- Inherently relies on mechanical accuracy.
- Materials limited to organics and metals

Directed assembly-based printing



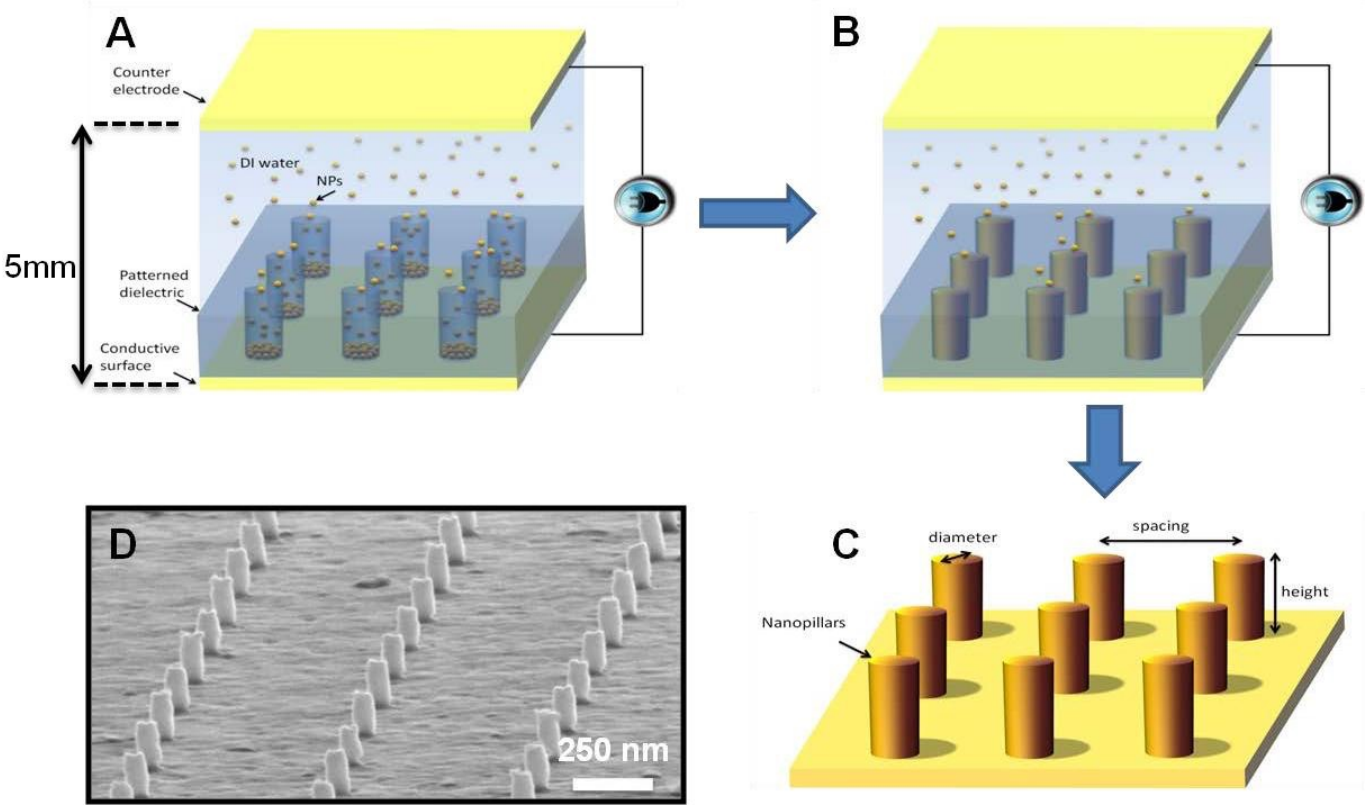


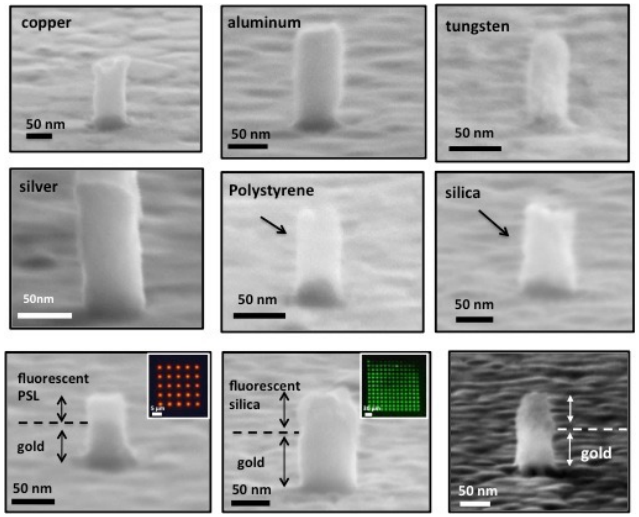
- **Directs each nanoparticle** (down to 3nm in size) toward a substrate to form a nanopattern.
- Prints 1000 times faster & smaller patterns than inkjets
- Prints one circuit layer per minute

NanoOPS©

Electrophoretic Directed Assembly– EPx Platform

Assembled Interconnects

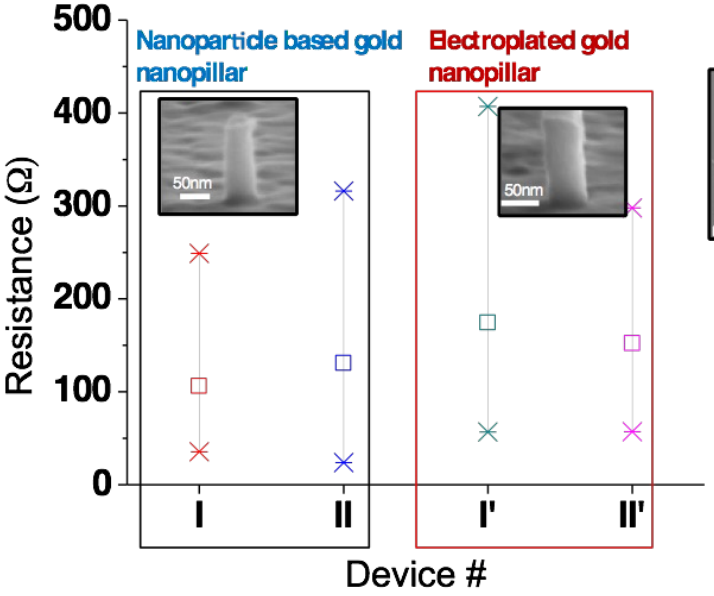


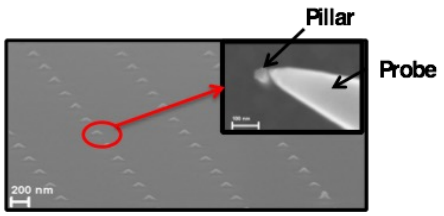


All assembled Nanoparticles are completely fused insitu.

ACS Nano, 8 (5), 2014.

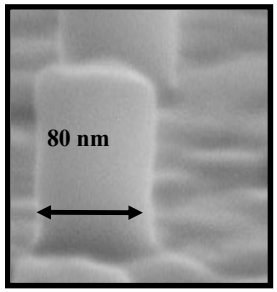
Interconnects Properties

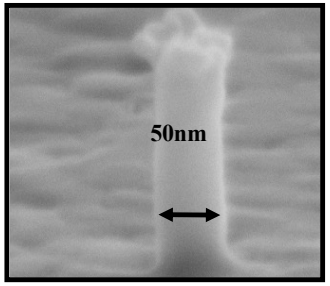


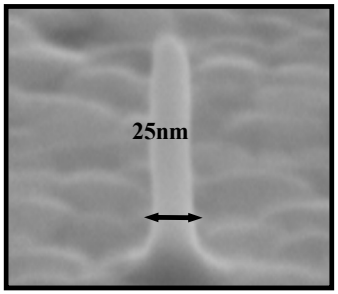


Resistance of assembled interconnects is the same as bulk (electroplated interconnects).

Crystalline Au Pillars





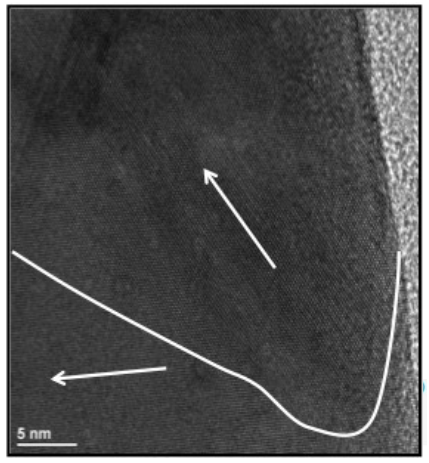


Directly assembled structures properties are equivalent to electroplating, CVD and PVD fabrication.

Directly assembled metallic structures (Cu, Ag, Al, Au, and W, etc.) in addition to semiconductors and dielectrics were demonstrated.

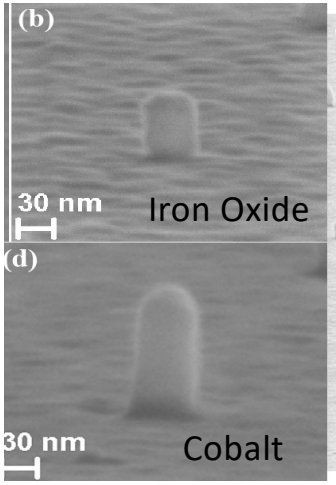
- TEM shows that NPs completely fuse without any voids at room temperature.
- Nanopillars have polycrystalline nature.

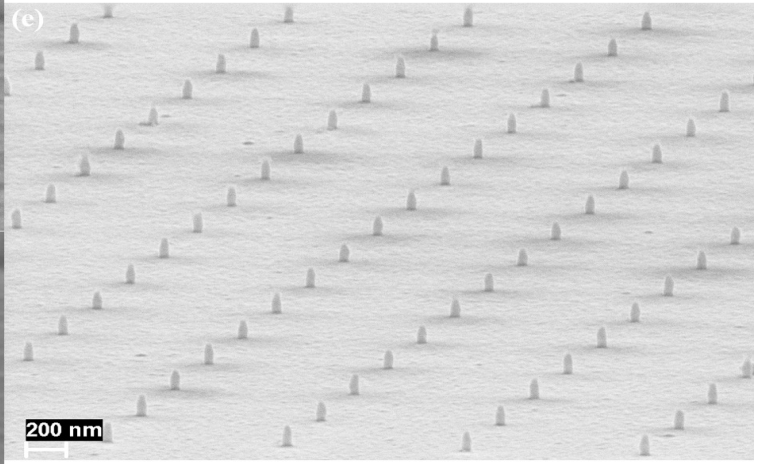
ACS Nano, 8 (5), 2014.

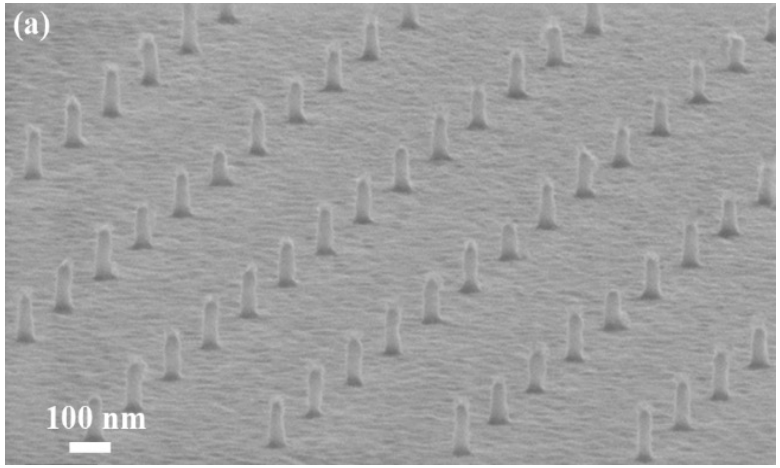


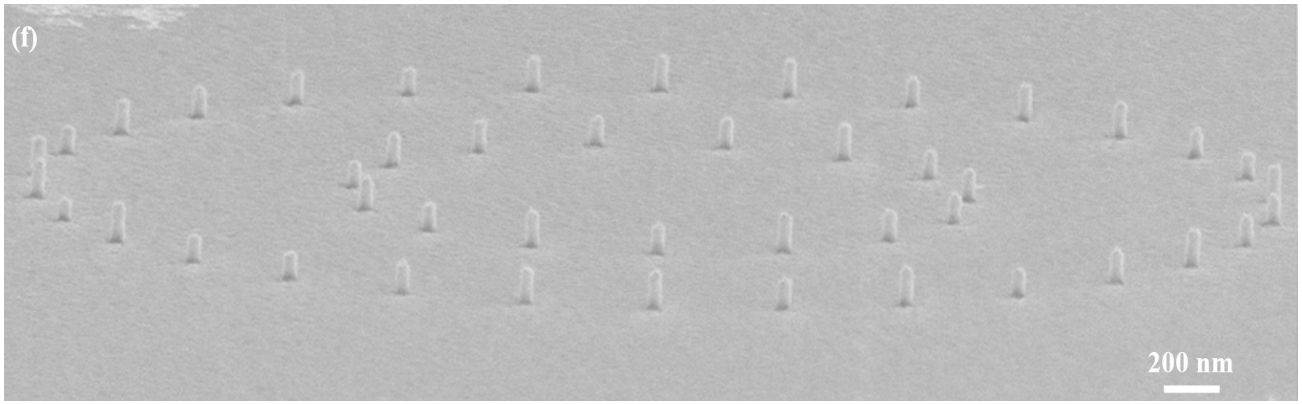
Printing 3D Nanostructures

Images of Printed nanorods using 20 nm silica nanoparticles.



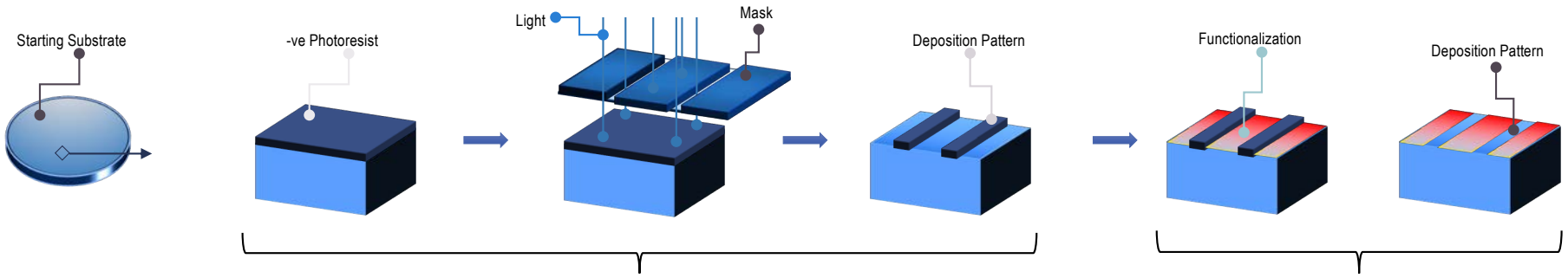


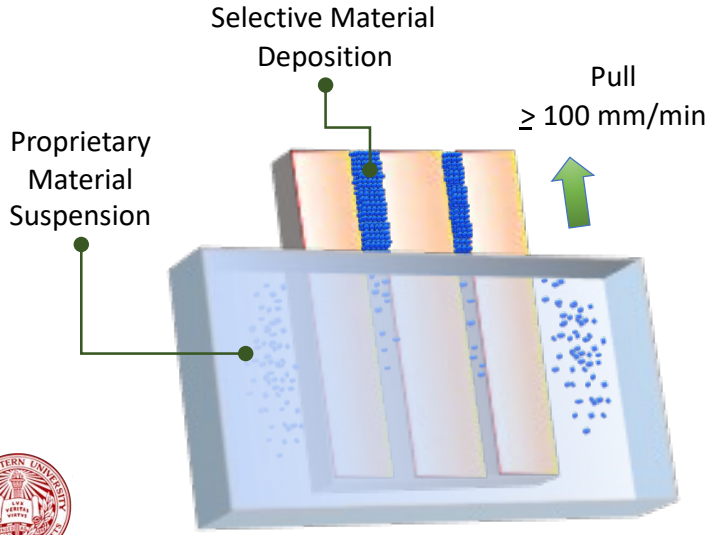


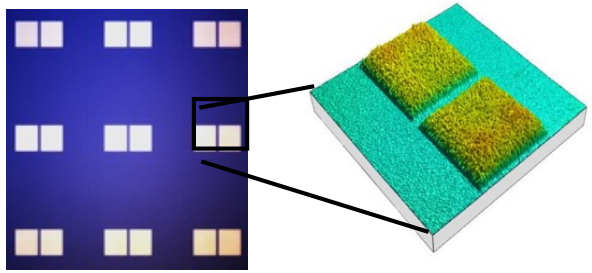


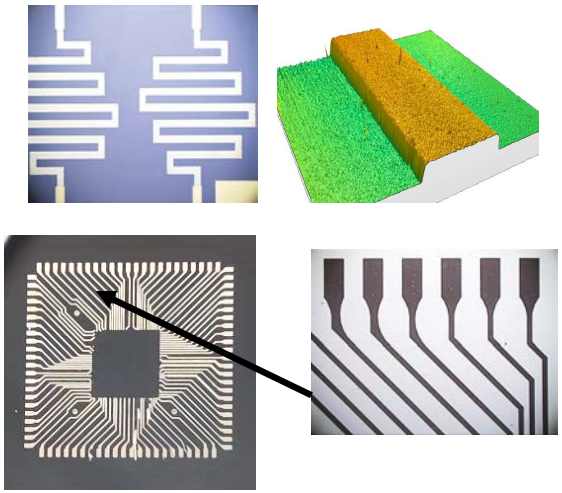
Nanotechnology, Volume 28, Number 47, November 2017.

Fast Fluidic Assembly Process– FFx Platform





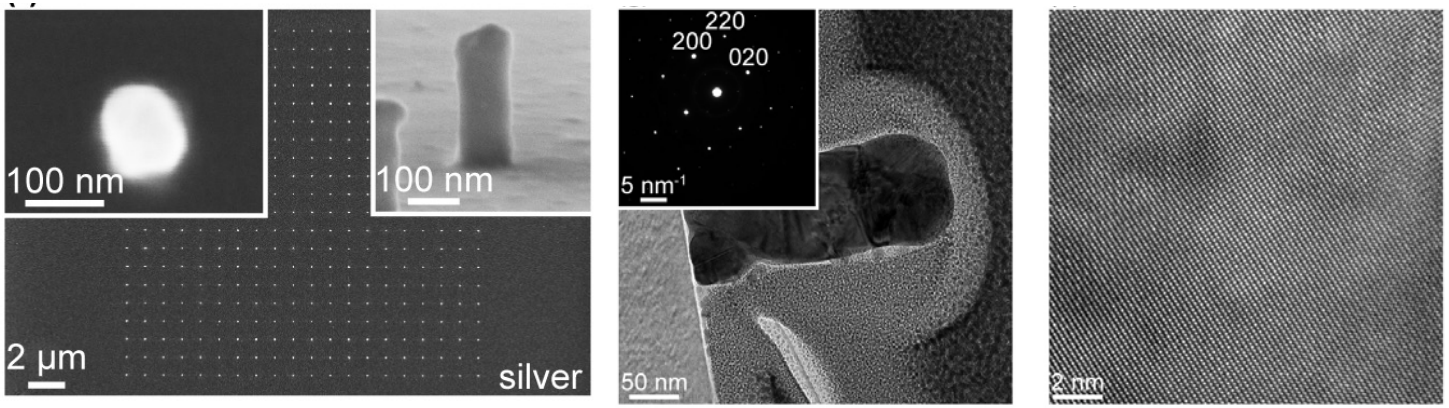




Fast Fluidic Assembly Process

Additively Manufacturing Single Crystal Semiconductor and Metal

Interfacial convective directed assembly

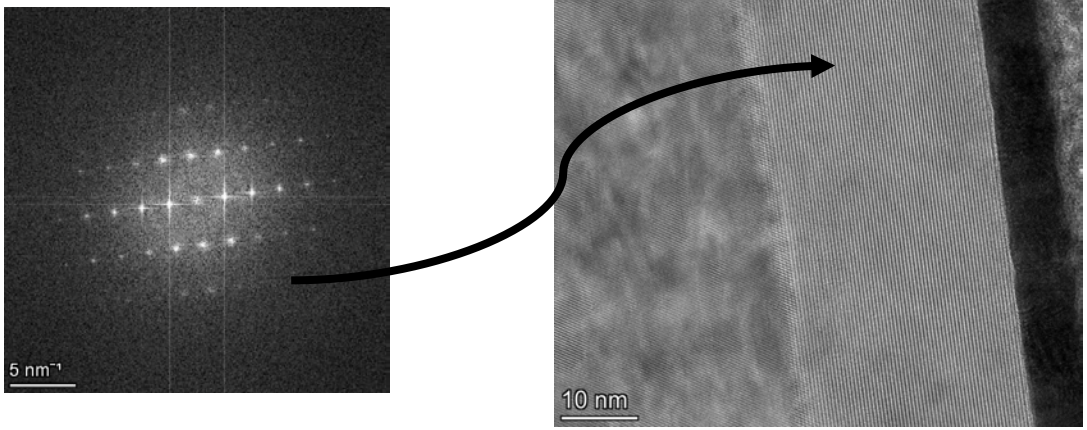


Advanced Materials, 2020.

Room temperature Printing & sintering to make wafer scale single crystal metal (Ag) nanostructures

Single Crystal TEM image of sintered assembled ZnO nanoparticles

Fast Fluidic directed assembly



RTP sintering of II-VI nanoparticles (1000 c for 2 min) on sapphire yields gives a single crystal structure throughout.

Directed Assembly for Nanoscale Devices Review Articles

ACSNANO

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REVIEW

Directed Assembly of Nanomaterials for Making Nanoscale Devices and Structures: Mechanisms and Applications

Zhimin Chai, Anthony Childress, and Ahmed A. Busnaina*

Cite This: https://doi.org/10.1021/acsnano.2c07910

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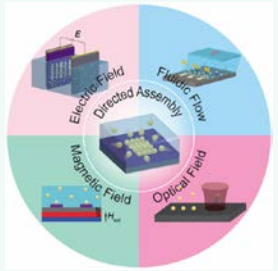
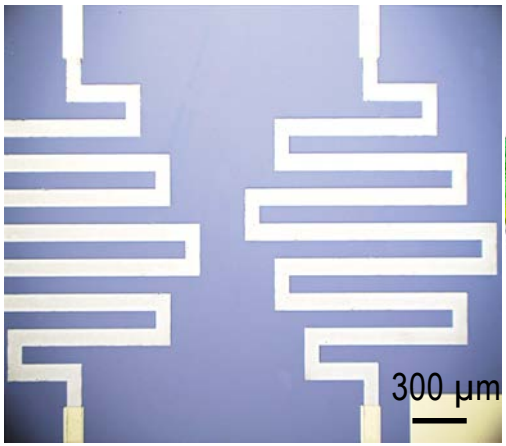
ABSTRACT: Nanofabrication has been utilized to manufacture one-, two-, and three-dimensional functional nanostructures for applications such as electronics, sensors, and photonic devices. Although conventional silicon-based nanofabrication (top-down approach) has developed into a technique with extremely high precision and integration density, nanofabrication based on directed assembly (bottom-up approach) is attracting more interest recently owing to its low cost and the advantages of additive manufacturing. Directed assembly is a process that utilizes external fields to directly interact with nanoelements (nanoparticles, 2D nanomaterials, nanotubes, nanowires, etc.) and drive the nanoelements to site-selectively assemble in patterned areas on substrates to form functional structures. Directed assembly processes can be divided into four different categories depending on the external fields: electric field-directed assembly, fluidic flow-directed assembly, magnetic field-directed assembly, and optical field-directed assembly. In this review, we summarize recent progress utilizing these four processes and address how these directed assembly processes harness the external fields, the underlying mechanism of how the external fields interact with the nanoelements, and the advantages and drawbacks of utilizing each method. Finally, we discuss applications made using directed assembly and provide a perspective on the future developments and challenges.

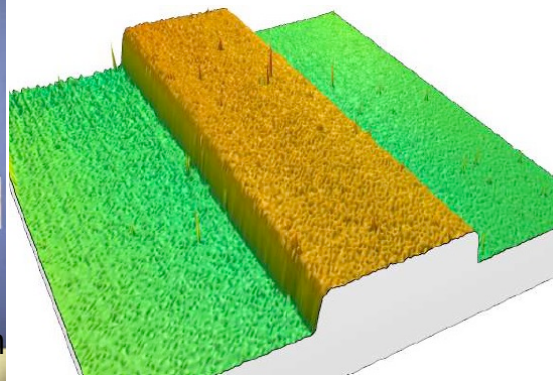


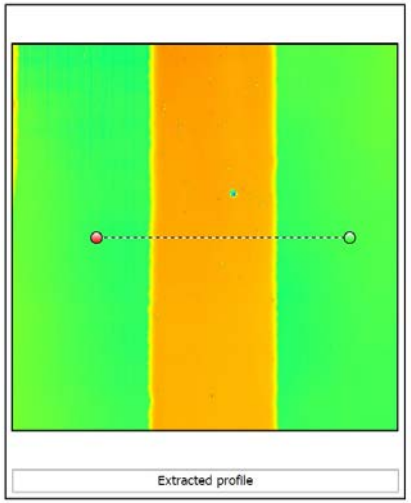
KEYWORDS: *directed assembly, bottom-up fabrication, nanomaterials, nanotechnology, nanoelectronics, microelectronics, electrophoresis, dielectrophoresis, magnetophoresis, fluidic assembly*

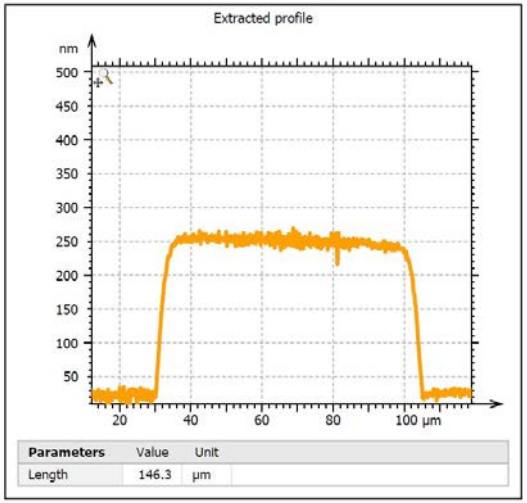
Profile of Metal Lines

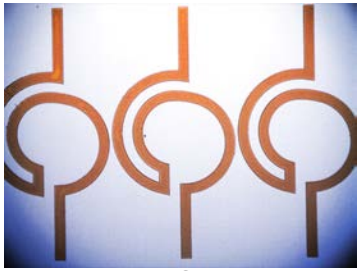
- Confocal microscope measurements show an average platinum thickness of 250 nm after annealing using RTP at 800 °C for 2 mins .

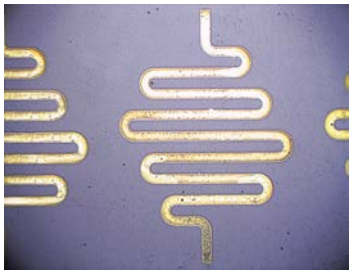


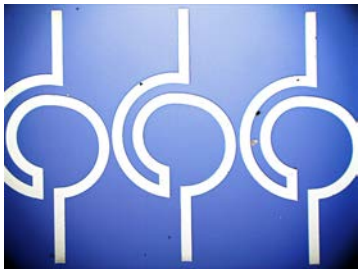







Copper


Gold

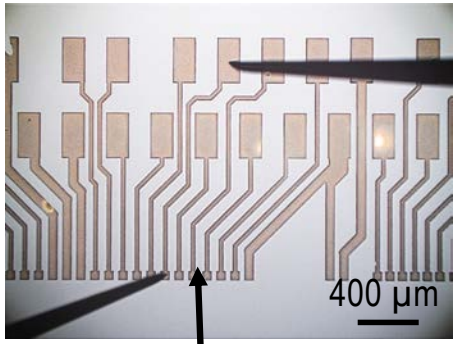

Platinum

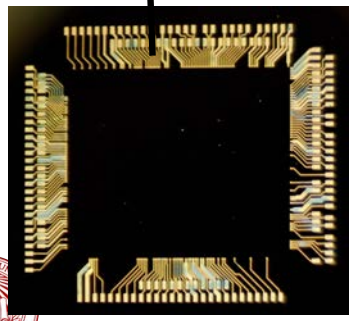
The printed Platinum shows uniform and homogeneous surface morphology.

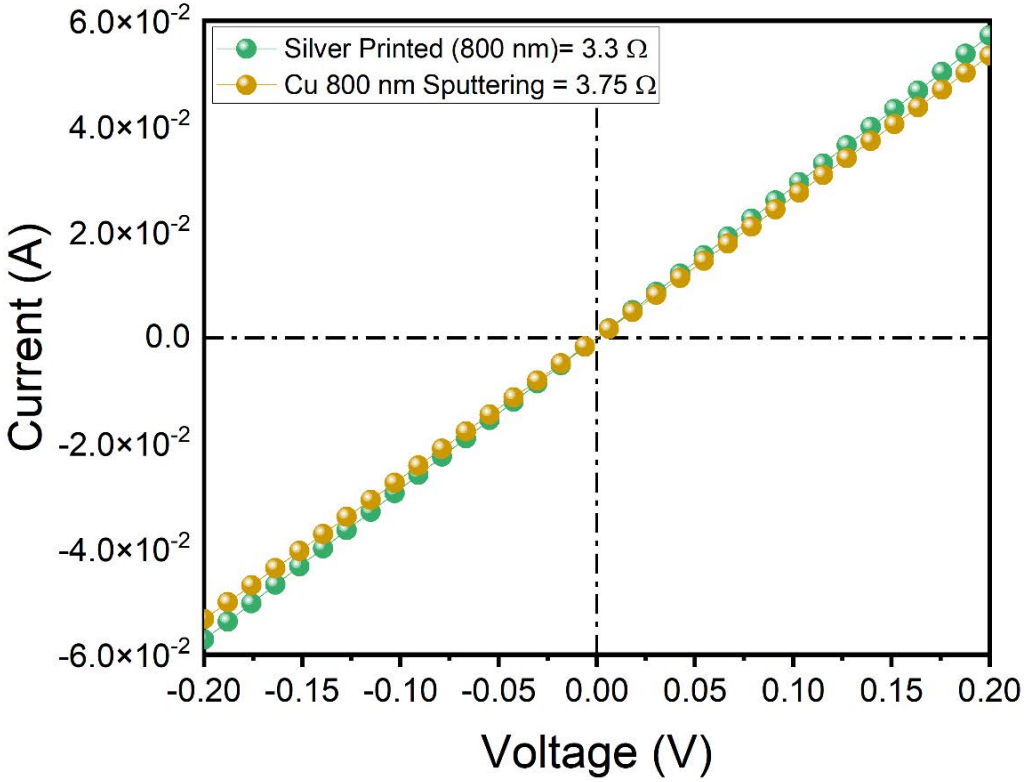
Additively Manufactured Silver vs Sputtered Copper

- Fan out Flip chip pattern was made using silver (internal pads < 40 microns)
- The trace's conductivity is equivalent to sputtered copper at the same thickness.

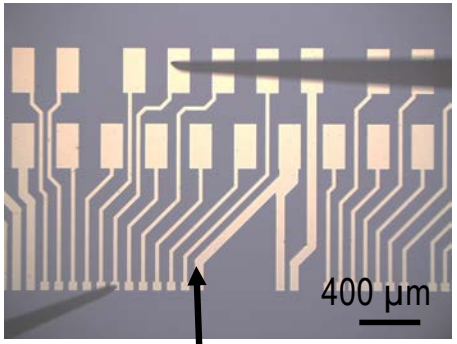
Silver

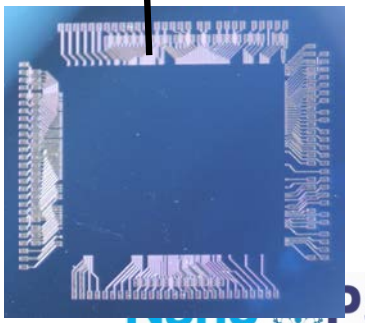




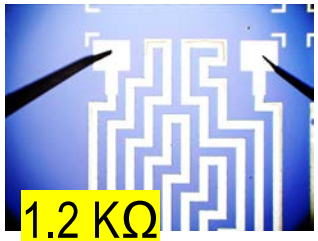


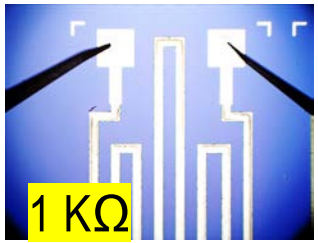
Copper (sputtered)

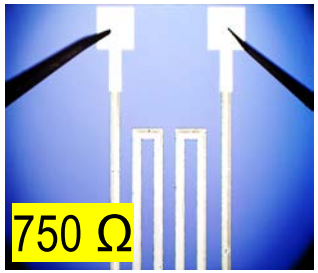


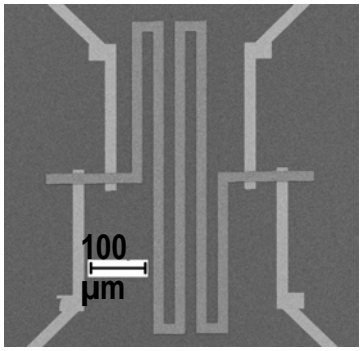


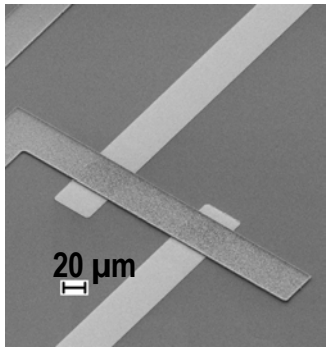
Additively Manufactured Components: Resistors

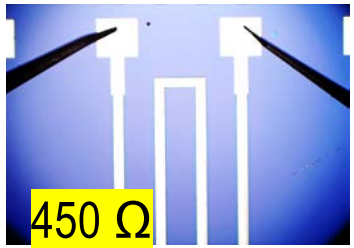


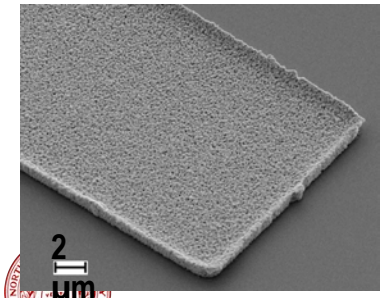


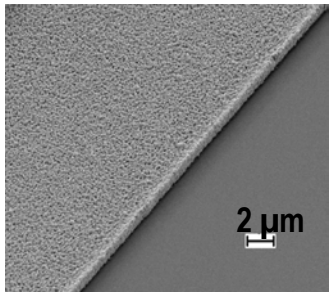


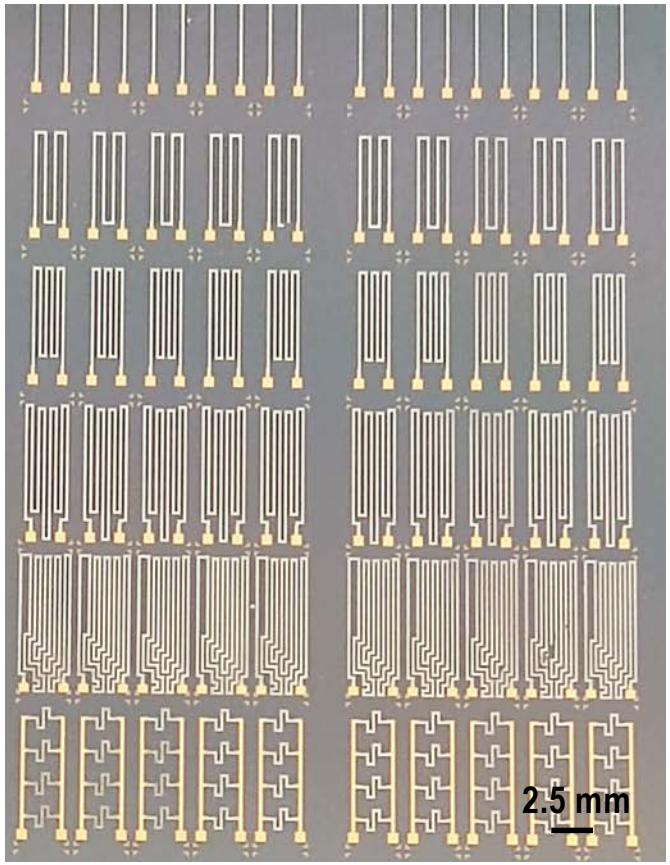












50 Ω

100 Ω

250 Ω

550 Ω

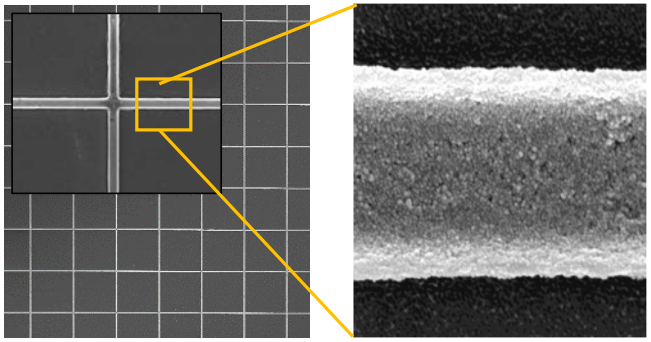
800 Ω

30 Ω

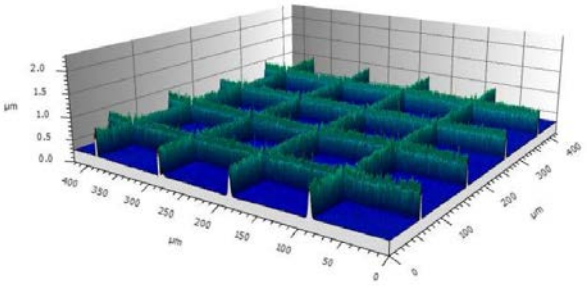
Thin metal film resistors

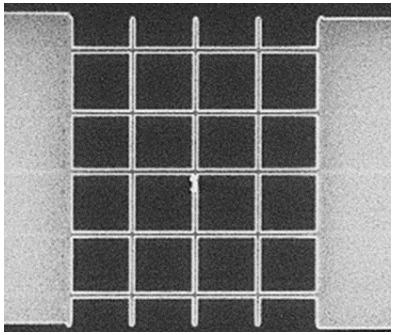
Additively Manufactured Touch Display at the Micro and Nanoscale

Ag grids for touch display applications

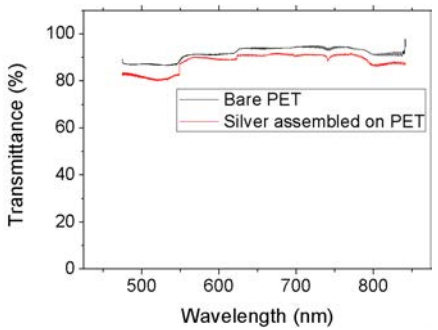


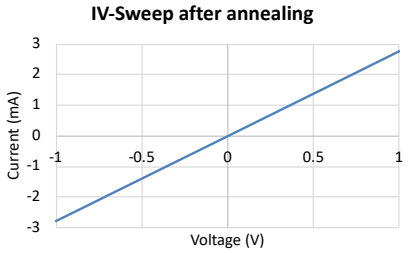
Line width 2 um





Line width 300 nm





COMMUNICATION

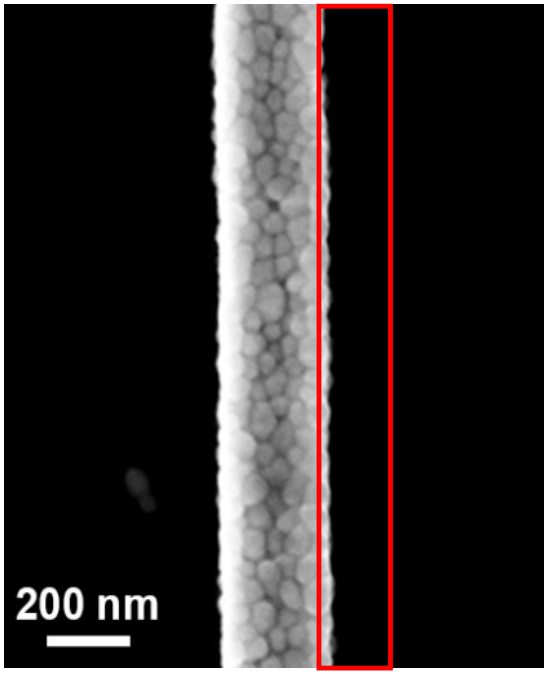
Transparent Electrodes

ADVANCED MATERIALS INTERFACES

www.advmatinterfaces.de

Scalable Printing of High-Resolution Flexible Transparent Grid Electrodes Using Directed Assembly of Silver Nanoparticles

*Salman A. Abbasi, Zhimin Chai, and Ahmed Busnaina**

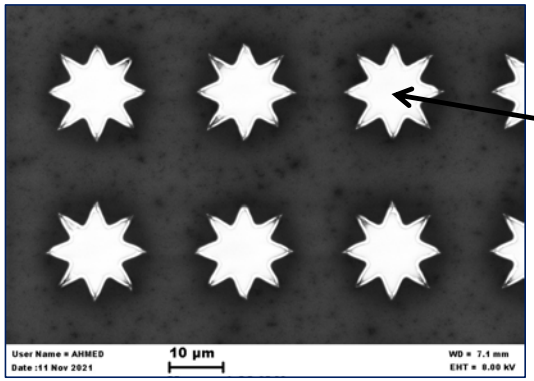


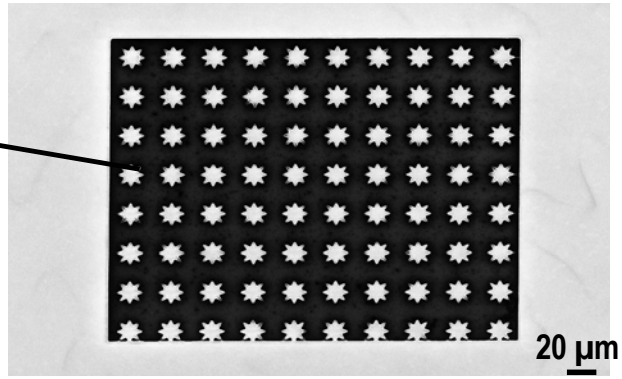
Excellent Line edge roughness
3.7 nm
Using large nanoparticles

Nano PS©

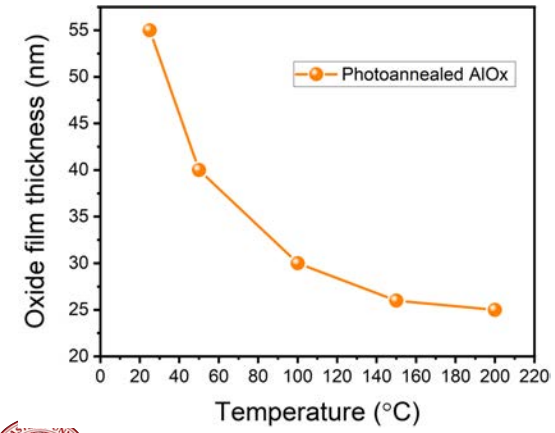
Additively Manufactured Dielectrics

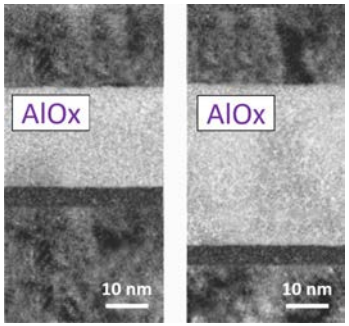
The SEM images below shows Al_2O_3 micropatterns prepared by directed fluidic assembly with a dielectric constant that matches that obtained by CVD or ALD ($\varepsilon_d = 7.2$).

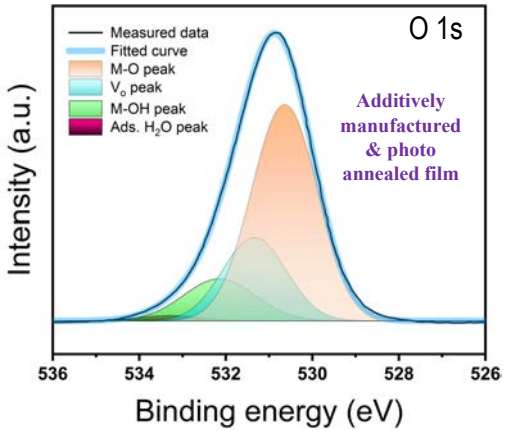


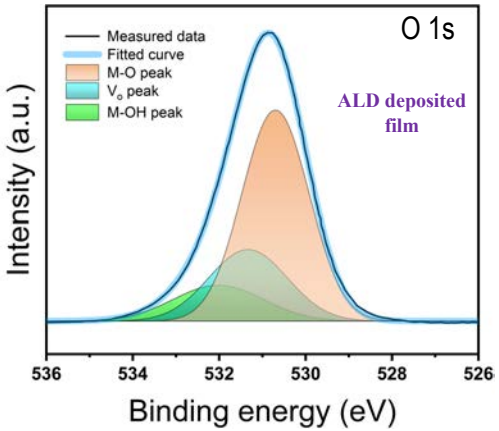


X-ray Photoelectron Spectroscopy (XPS) characterization of the Dielectric Layer shows agreement in between ALD and printed films in terms of peak intensities and composition ratios.







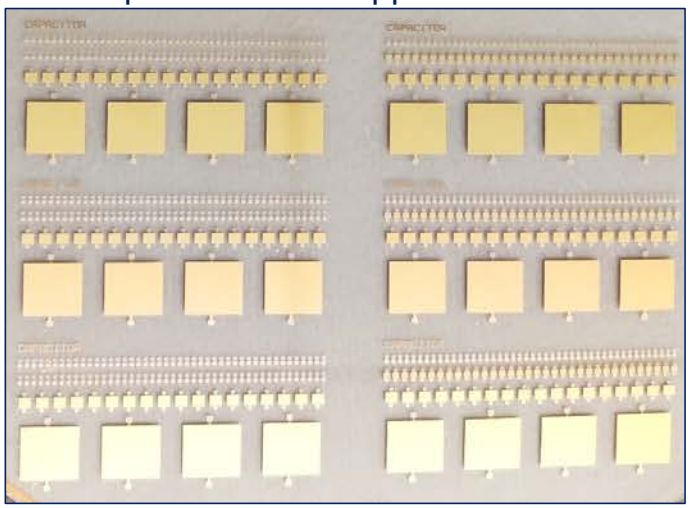


- Higher temperature densification and better dielectric properties for the film.
- Cross-sectional shows the oxide film thickness variation between 50 °C and 200 °C annealing.

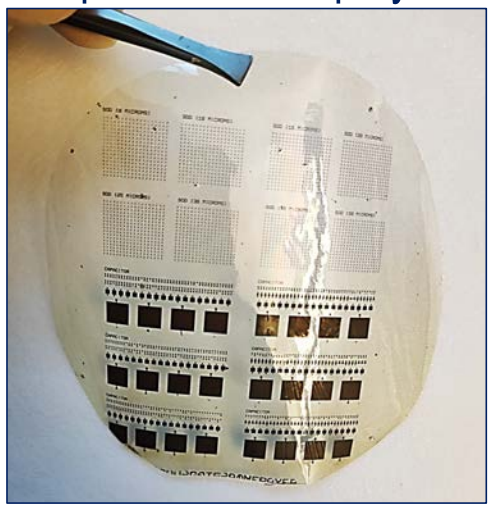
Additively Manufactured Capacitors on Rigid and Flexible Substrates

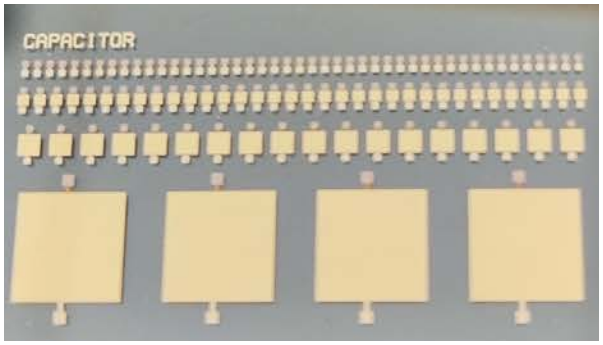
- Large-scale fabricated capacitors with a dielectric layer onto sapphire or polymer substrates.
- Each substrate has 640 capacitors with different surface areas of side lengths 20, 50, 100, 500, 1000, and 5000 µm.
- Metal: **Silver**
- Dielectrics: **Al_2O_3, SiO_2, HfO_2**

Capacitors on a sapphire substrate

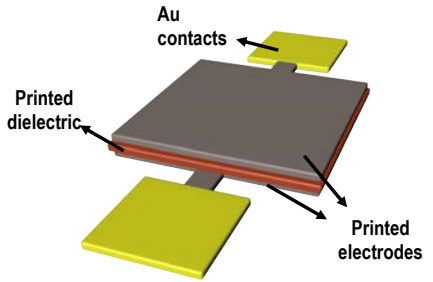


Capacitors on a polymer





Capacitors on silicon



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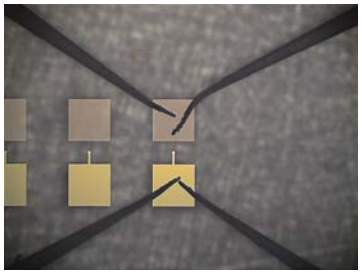
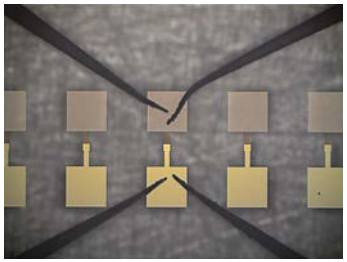
Characterization of Additively Manufactured Capacitors

- For high-frequency applications, the capacitors need to show reliable performance under high frequency.
- The curve shows the capacitance variation versus different frequencies up to 1 MHz.



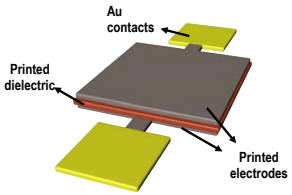
20x20 µm

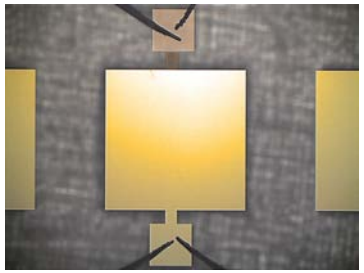
C= 857 fF



50x50 µm

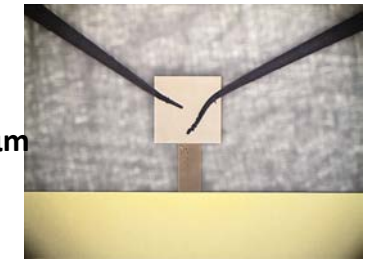
C= 4.3 pF





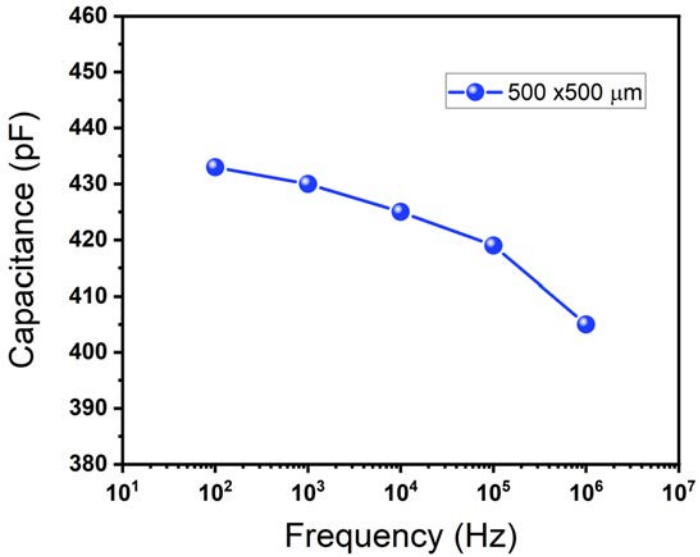
1000x1000 µm

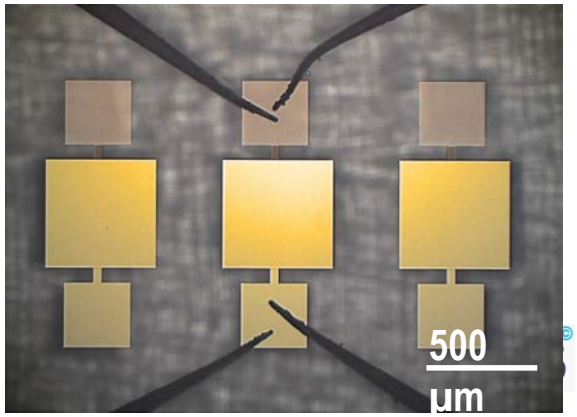
C= 1.6 nF



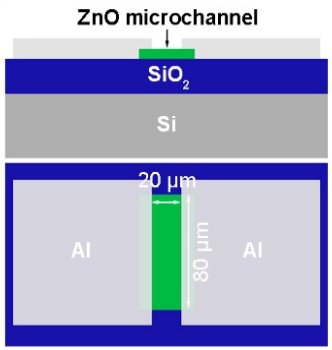
5000x5000 µm

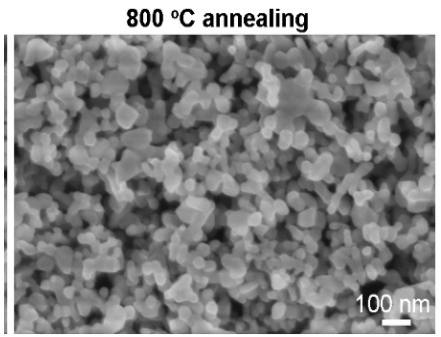
C= 5.68 nF

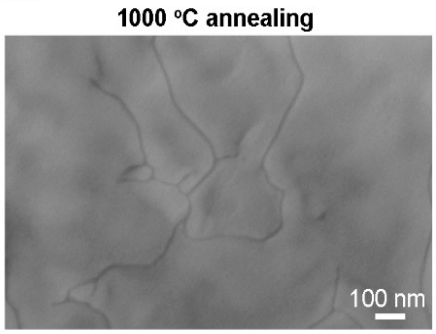


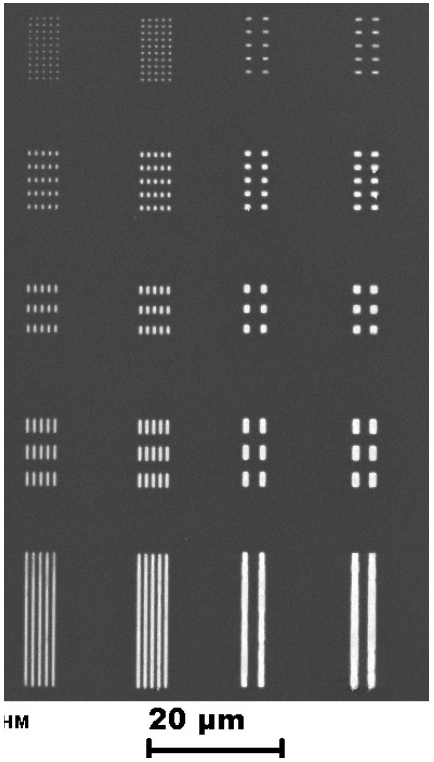


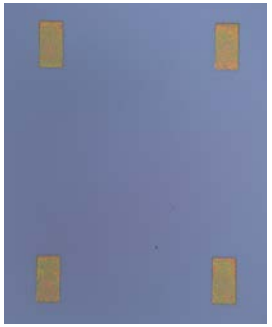
Field Effect Transistor (FET) Using II-VI Semiconductors



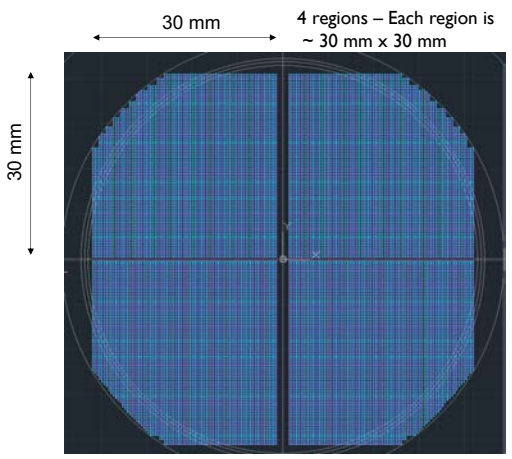


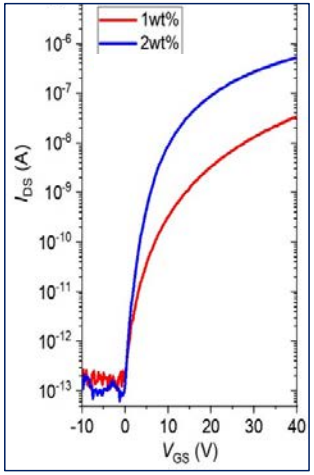






Channel width varied from 100 nm to 2 um, length varied from 100 nm to 20 um

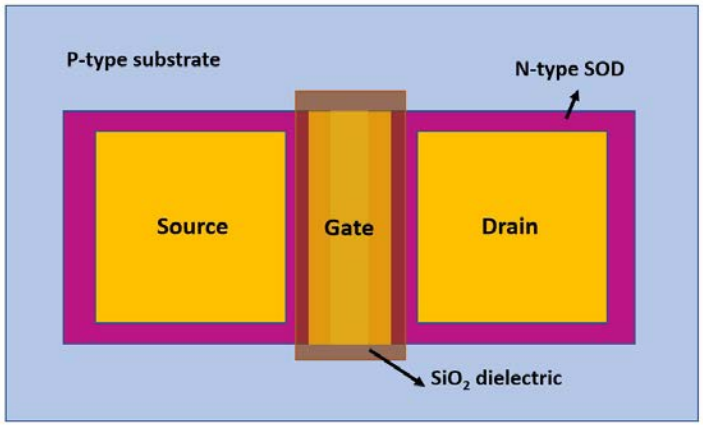




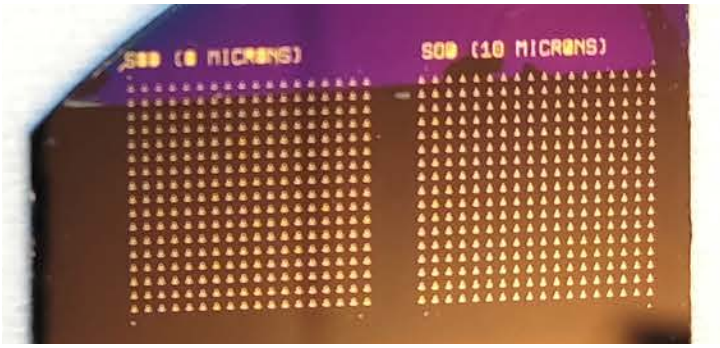
Wafer-level manufacturing of 37,000 transistors exhibiting an on/off ratio higher than 10^6 after annealing.

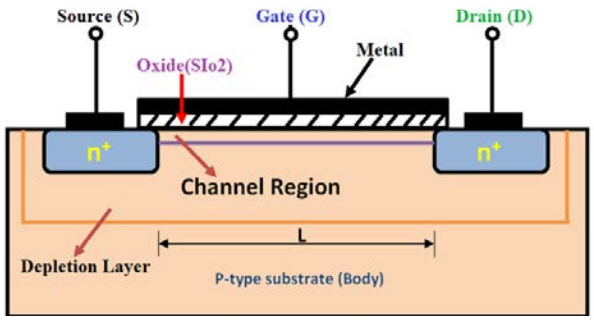
ACS Applied Electronic Materials, 2023

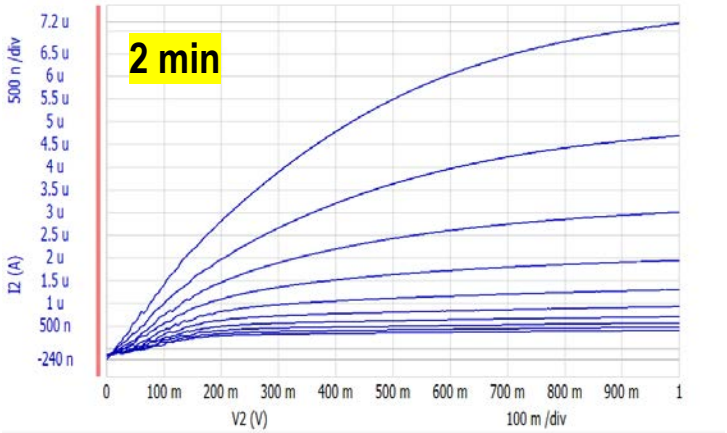
Additively Manufactured Silicon Transistors (MOSFETs)

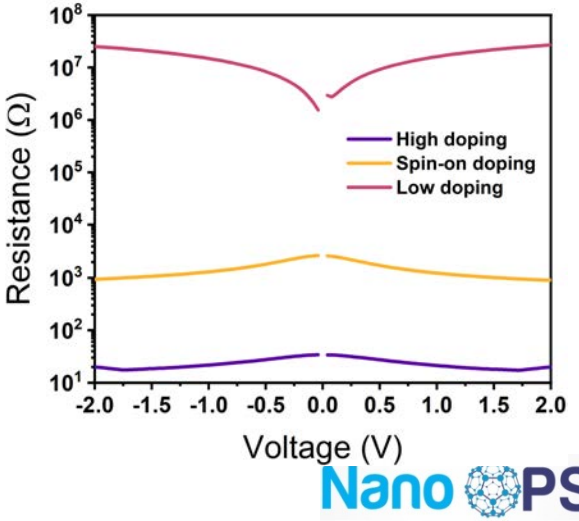


A fully additive liquid-based process process to manufacture MOSFETs using dopants inks.









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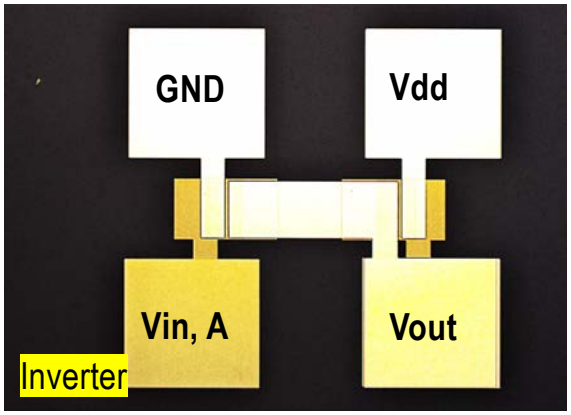
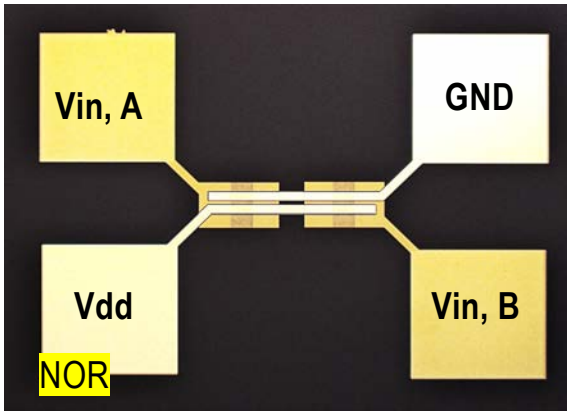
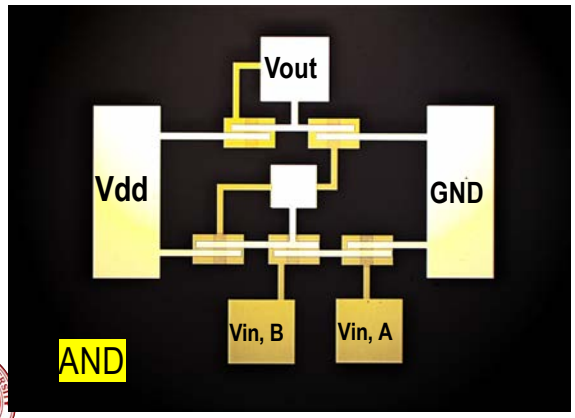
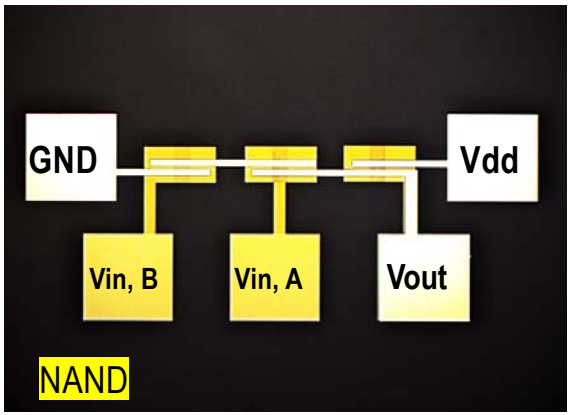
Additively Manufactured Logic Gate Electronics

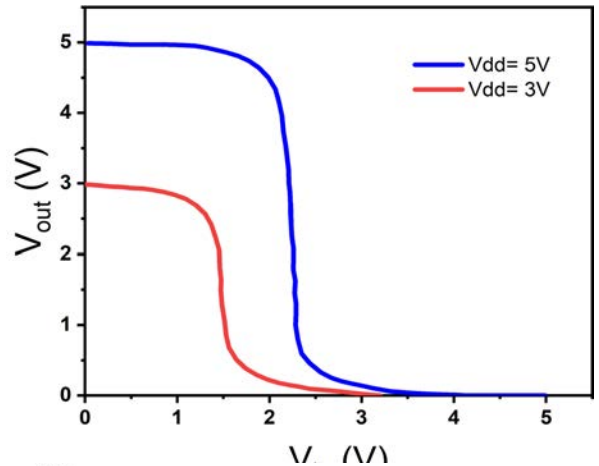
- Logic gates such as Inverters, AND, NAND, and NOR were printed
- The figures below show the fabricated logic circuits

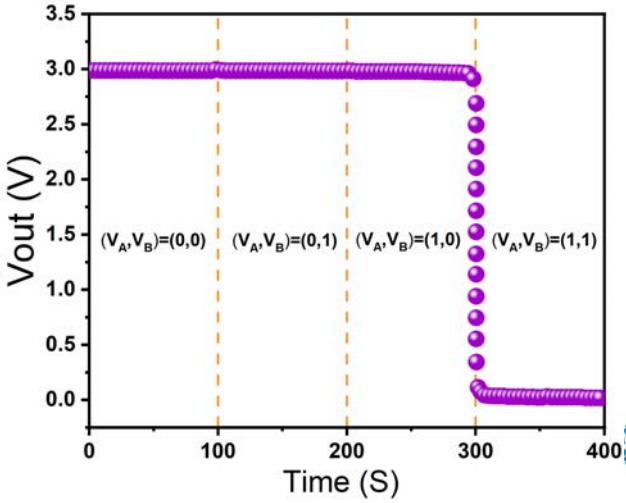




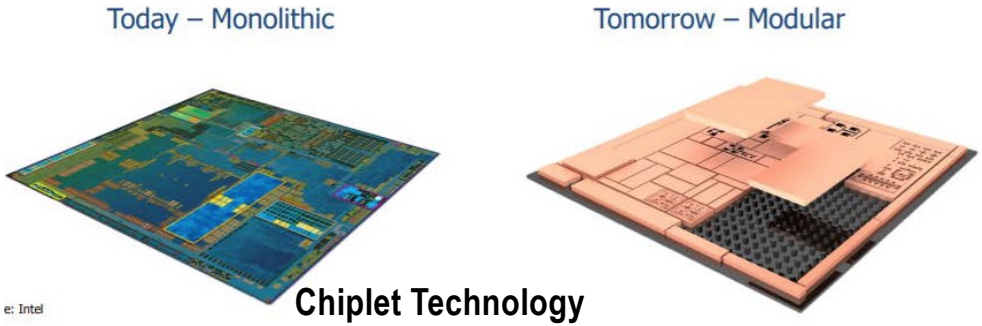








Advanced Packaging for Heterogeneous Integration
for chiplet technology for integrating multiple dies in a package or system



Chiplet Technology

- **Conventional packaging approaches can not meet the resolution and density requirements.**
- **It can only be done at conventional fabs now.**

Fully automated and cyber enabled system

- **Submit DXF or GDS files and load ink, wafers, etc.**
- **Additively Manufacture:**
  - **micro and submicron interconnects.**
  - **passive components**
  - **onto silicon, glass or organic substrates (interposers)**

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The Future of Electronics Manufacturing

Any Material
Any Substrate

Minimum Feature Size
20 nm

High throughput
10 – 100x Faster

Cheaper 10 – 100x

Fab-in-a-Tool: A Fully Automated Nanoscale Electronics Manufacturing Platform

https://www.youtube.com/watch?v=QpbDfAJzXDU&t=7s

www.nano-ops.us

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Technological Impact

- Adv. Packaging on demand
- Passive and Active components on demand
- Fast prototyping and development cycle
- Security
- Sustainable
- Material innovation